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A NOVEL SWITCHING PATTERN OF CASCADED MULTILEVEL INVERTERS FED BLDC DRIVE USING DIFFERENT MODULATION SCHEMES

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ABSTRACT

Use of multilevel inverters has become popular in recent years for high-power applications. Various topologies and modulation strategies have been investigated for utility and drive applications in the literature. The THD contents in output voltage of inverters is very significant index as the performance of drive depends very much on the quality of voltage applied to drive. The THD depends on the switching angles for different units of multilevel inverters; therefore, the switching angles are calculated first by using N-R method where certain number of harmonic components has been eliminated. In this paper multilevel converter fed BLDC drive with different voltage levels are considered and simulation results are presented in terms of total harmonic distortion (THD). The simulations have been carried out in MATLAB and Simulink.

KEYWORDS: Cascaded H-Bridge (CHB) Multilevel Inverter (MLI), Total Harmonic Distortion (THD), Pulse Width Modulation (PWM), Switching Frequency, BLDC Drive

INTRODUCTION

Recent advances in the power-handling capabilities of static switch devices such as IGBTs with voltage rating up to 4.5 kV commercially available, has made the use of the voltage source inverters (VSI) feasible for high-power applications. High power and high-voltage conversion systems have become very important issues for the power electronic industry handling the large ac drive and electrical power applications at both the transmission and distribution levels. For these reasons, a new family of multilevel inverters has emerged as the solution for working with higher voltage levels. Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc voltage sources. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output; however, the rated voltage of the power semiconductor switches depends only upon the rating of the dc voltage sources to which they are connected.

A two-level inverter generates an output voltage with two values (levels) with respect to the negative terminal of the capacitor Figure 1(a), while the three-level inverter generates three voltages, and so on.

The term multilevel starts with the three-level inverter introduced by Nabaeet al. By increasing the number of levels in the inverter, the output voltages have more steps generating a staircase waveform, which has a reduced harmonic

distortion [4], [5]. However, a high number of levels increases the control complexity and introduces voltage imbalance problems. Three different topologies have been proposed for multilevel inverters: diode-clamped or neutral point clamped, flying capacitors clamped and cascaded multi cell with separate dc sources. In addition, several modulation and control strategies have been developed or adopted for multilevel inverters including the following: multilevel sinusoidal pulse width modulation (SPWM).

A multilevel converter has several advantages over a conventional two-level converter that uses high switching frequency pulse width modulation (PWM) [6],[7],[8].

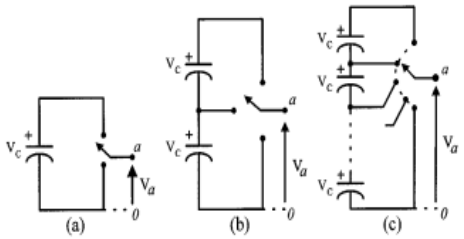

Figure 1: One Phase Leg of an Inverter with (a) Two Levels, (b) Three Levels, and (c) N Levels

There are different approaches for the selection of switching techniques for the multilevel inverters. Finally a seven level CHB inverter with phase shifted carrier is applied for BLDC drive and simulation results are presented.

BRUSHLESS DC MOTOR (BLDC MOTOR)

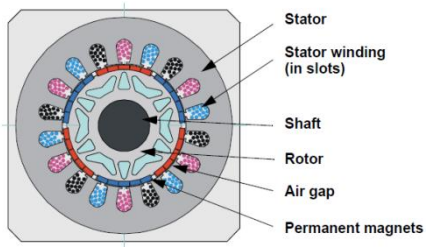

Figure 2: BLDC Motor/Cross Section

The brushless DC motor (BLDC motor) is a rotating electric machine with a classic three-phase stator similar to an induction motor; the rotor has surface-mounted permanent magnets. It is also referred to as an electronically commuted motor. There are no brushes on the rotor and the commutation is performed electronically at certain rotor positions. The stator is usually made from magnetic steel sheets. Figure-2shows a typical cross section of BLDC motor. The stator phase windings are inserted in the slots (distributed winding) or it can be wound as one coil on the magnetic pole. Because the air gap magnetic field is produced by permanent magnets, the rotor magnetic field is constant. The magnetization of the permanent magnets and their displacement on the rotor is chosen so that the back-EMF (the voltage induced into the stator winding due to rotor movement) shape is trapezoidal. This allows the DC voltage (Figure-3), with a rectangular shape, to create a rotational field with low torque ripples.

The motor can have more than one pole-pair per phase. The pole-pair per phase defines the ratio between the electrical revolution and the mechanical revolution. For example, the shown BLDC motor has three pole-pairs per phase that represent the three electrical revolutions per one mechanical revolution. The rectangular shape of applied voltage ensures the simplicity of control and drive. However, the rotor position must be known at certain angles to align the applied voltage with the back-EMF. The alignment between back-EMF and commutation events is important. At this

condition, the motor behaves as a DC motor and runs at the best working point. Therefore, simplicity of control and performance makes the BLDC motor the best choice for low-cost and high-efficiency applications.

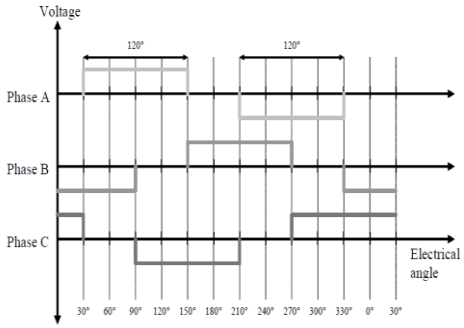

Figure 3: Three Phase Voltage System for BLDC Motor

CASCADED H-BRIDGE MULTILEVEL INVERTER

A single-phase structure of an m-level cascaded inverter is illustrated in Figure 4. Each separate dc source (SDCS) is connected to a single-phase full-bridge, or H-bridge, inverter. Each inverter level can generate three different voltage outputs, +Vdc, 0, and –Vdc by connecting the dc source to the ac output by different combinations of the four switches, S1, S2, S3, and S4. To obtain +Vdc, switches S1 and S4 are turned on, whereas –Vdc can be obtained by turning on switches S2 and S3. By turning on S1 and S2 or S3 and S4, the output voltage is 0. The ac outputs of each of the different full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels m in a cascade inverter is defined by m = 2s+1, where s is the number of separate dc sources. An example phase voltage waveform for an 7-level cascaded H-bridge inverter with 3 SDCSs and 3 full bridges is shown in Figure 5. The phase voltage van = va1 + va2 + va3.

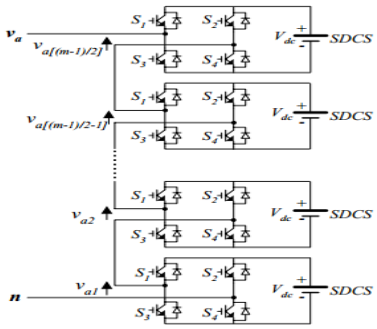

Figure 4: Single-Phase Structure of a Multilevel Cascaded H-Bridges Inverter

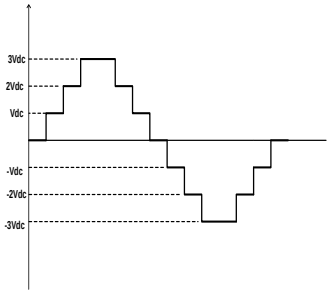

Figure 5: Output Phase Voltage Waveform of an 7-Level Cascade Inverter with 5 Separate Dc Sources

Advantages

- The number of possible output voltage levels is more than twice the number of dc sources (m = 2s + 1).

- The series of H-bridges makes for modularized layout and packaging. This will enable the manufacturing process to be done more quickly and cheaply.

Disadvantages

Separate dc sources are required for each of the H-bridges. This will limit its application to products that already have multiple SDCSs readily available.

MULTICARRIER PULSE WIDTH MODULATION TECHNIQUES

The carrier based PWM techniques for cascaded multilevel inverter can be broadly classified into: phase shifted modulation and level shifted modulation. In both the techniques, for an m level inverter, (m-1) triangular carrier waves are required. And all the carrier waves should have the same frequency and the same peak to peak magnitude.

Phase Shifted Multicarrier Modulation

In phase shifted PWM (PSCPWM), there is a phase shift of between the adjacent carrier signals. For a three phase inverter, the modulating signals should also be three phase sinusoidal signals with adjustable magnitude and frequency. The frequency modulation index and the amplitude modulation index .The amplitude modulation lies in the range of 0 to 1.

Level Shifted Multicarrier Modulation

In Level Shifted PWM (LS –PWM), the triangular waves are vertically displaced such that the bands occupy are contiguous. The amplitude modulation lies in the range of 0 to 1.

IMPLEMENTATION OF CASCADED H- BRIDGE CONVERTER

Full H-Bridge- Three Level Inverter

Figure 6 shows the Full H-Bridge Configuration. By using single H-Bridge we can get 2 and 3 voltage levels. The number output voltage levels of cascaded Full H-Bridge inverter are given by 2n+1 and voltage step of each level is given by Vdc/n. Where n is number of H-bridges inverter connected in cascaded. The switching table is given in Table 1and 2.

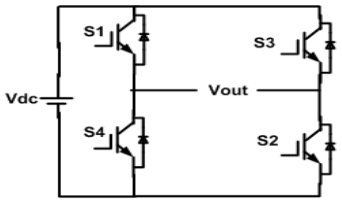

Figure 6: Full H-Bridge Inverter

Table 1: Switching Table for Full H-Bridge Inverter

Switches Turn ON	Voltage Level
S1,S2	Vdc/2
S3,S4	-Vdc/2

Table 2: Shows the Switching Table for Full H-Bridge for Three Level Inverter

Switches Turn ON	Voltage Level
S1,S2	VDC/2
S3,S4	-VDC/2
S2,S4	0

Five Level CHB Inverter

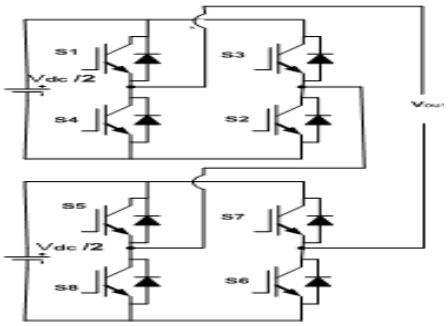

Figure 7: Five Level CHB Inverter

Figure 7 Shows the five level multilevel inverter and Table III shows the switching states of the 5 level inverter. Here even though we have eight switches at any switching state only two switches are on/off at a voltage level of Vdc/2, so switching losses are reduced. In three level inverter dv/dt is Vdc, but in five level inverter dv/dt is Vdc/2. As dv/dt reduces the stress on switches reduces and EMI reduces.

Table 3: Switching Table for Full H-Bridge of Five Level Inverter

Switches Turn ON	Voltage Level
S1,S2,S6,S8	Vdc/2
S1,S2,S5,S6	Vdc
S2,S4,S6,S8	0
S3,S4,S6,S8	-Vdc/2
S3,S4,S6,S8	-Vdc

Seven Level CHB Inverter

Figure 8 Shows the seven level multilevel inverter and Table IV shows the switching states of the seven level CHB inverter.,,

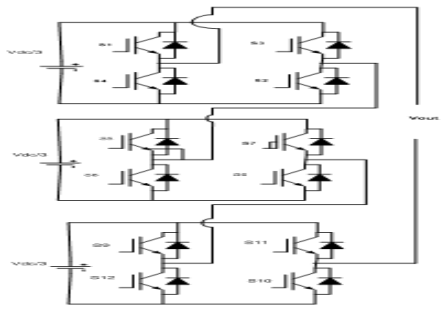

Figure 8: Seven Level CHB Inverter

Table 4: Switching Table for Full H-Bridge of Seven Level Inverter

Switches Turn ON	Voltage Level
S1,S2,S6,S8,S10,S12	Vdc/3
S1,S2,S6,S8,S10,S12	2Vdc/3
S1,S2,S5,S6,S9,S10	Vdc
S2,S4,S6,S8,S10,S12	0
S3,S4,S6,S8,S10,S12	-Vdc/3
S3,S4,S6,S8,S10,S12	-2Vdc/3
S3,S4,S7,S8,S11,S12	-Vdc

MATLAB MODELEING AND SIMULATION RESULTS

Case1

Cascaded H-bridge Multi level Inverter (seven level) Fed BLDC Motor Employing Phase shifted carrier PWM technique

The following figure 9 shows the Matlab/simulink diagram of BLDC Motor which is fed from the Cascaded H-bridge Multi level Inverter Using Phase shifted carrier PWM techniques (PSCPWM).

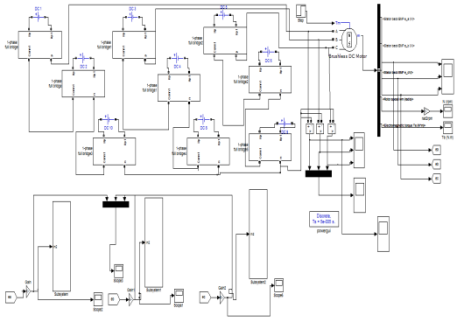

Figure 9: Matlab/Simulink Circuit of the Phase Shifted MLI FED BLDC Motor

The following figure 10 shows the three phase voltages of the MLI, which are displaced by 120 degrees apart.

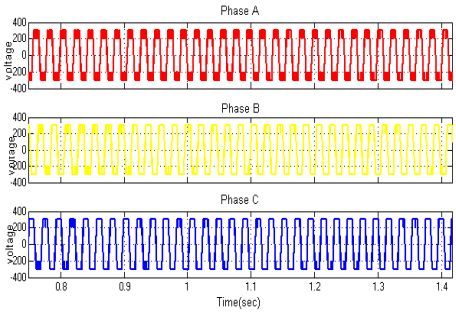

Figure 10: Phase Voltages of Phase Shifted Multi Level Inverter

The following figures 11, 12 and figure 13 represents the Back emf, speed and Electromagnetic torque of the BLDC motor respectively.

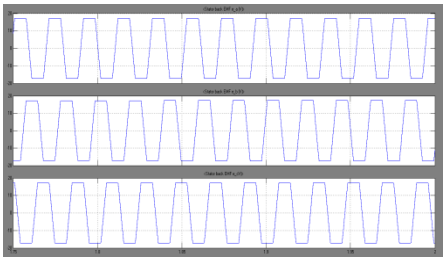

Figure 11: Back Emf's of the BLDC Motor

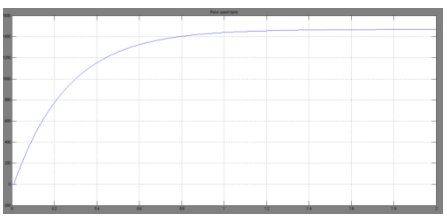

Figure 12: Speed of the BLDC Motor

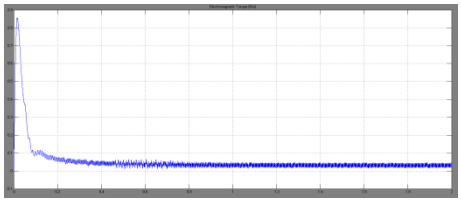

Figure 13: Electromagnetic Torque of the BLDC Motor

THD of the Cascaded H-bridge Multilevel Inverter Employing Phase shifted carrier PWM technique is shown in figure 14 and it is equal to 21.31%.

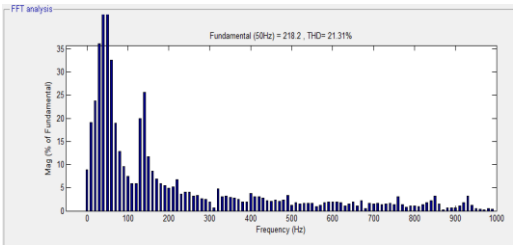

Figure 14: THD of the Phase Shifted MLI (Seven Level) Output Voltage

Case 2

Cascaded H-bridge Multi level Inverter (seven level) Fed BLDC Motor Employing Level shifted carrier PWM technique

The following figure 15 shows the three phase voltages of the MLI, which are displaced by 120 degrees apart.

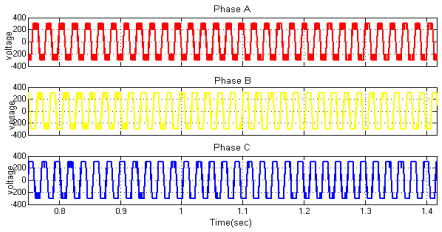

Figure 15: Phase Voltages of Level Shifted Multi Level Inverter

The following figures 16, 17 and figure 18 represents the Back emf, speed and Electromagnetic torque of the BLDC motor respectively.

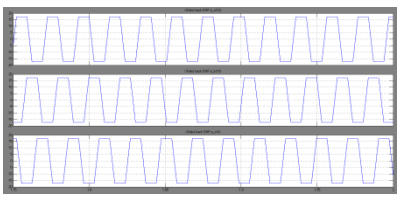

Figure 16: Back Emf's of the BLDC Motor

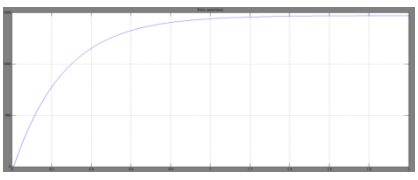

Figure 17: Speed of the BLDC Motor

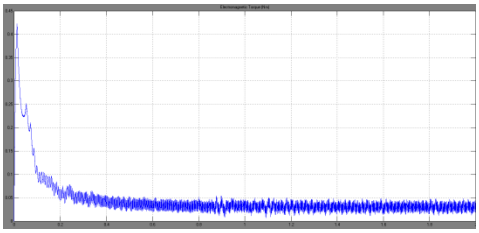

Figure 18: Electromagnetic Torque of the BLDC Motor

THD of the Cascaded H-bridge Multilevel Inverter Employing Level shifted carrier PWM technique is shown in figure 19 and it is equal to 19.13%.

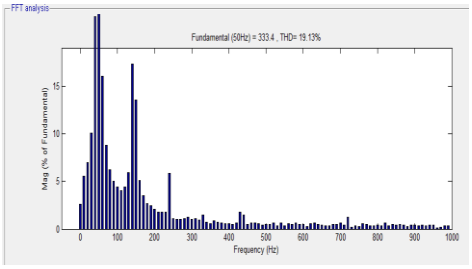

Figure 19: THD of the Level Shifted MLI (Seven Level) Output Voltage

CONCLUSIONS

The use of a permanent-magnet (PM) brushless dc motor (PMBLDCM) in low-power appliances is increasing because of its features of high efficiency, wide speed range, and low maintenance. It is a rugged three phase synchronous motor due to the use of PMs on the rotor. The commutation in a PMBLDCM is accomplished by solid state switches of a three phase voltage source Inverter (VSI). Its application to a fan results in an improved efficiency of the system if operated under speed control. The basic structure and operating characteristics of cascaded multilevel inverter have been changed by using different pwm techniques. The inverter cell is low means the design of the inverter switch pattern is easiest. Multilevel inverter is to obtain a high resolution. The technique is used to improve the level of the inverter and extends the design flexibility and reduces the harmonics. A SPWM approach was presented to deal with the uneven power transferring characteristics of the conventional SPWM modulation techniques. Base to THD analyze for two different modulation techniques we have also highlighted that at seven-level and the harmonics are very low.

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